Attorney Docket No. P15753

IN THE CLAIMS:

1-4 (cancelled)

5. (currently amended) A method for supporting at least a first and second power state comprising:

generating a first Phase Locked Loop(PLL) clock for a first power state;

generating a second Phase Locked Loop clock for a second power state; [and]

adjusting a voltage and a frequency of a processor based at least in part on the first or second power state[.] ; and

changing a frequency of the first Phase Locked Loop clock within a single clock cycle based on a processor utilization and changing a frequency of the second Phase Locked Loop clock after a completion of a PLL relock.

6-14 (cancelled)

15. (currently amended) An system comprising:

a processor with an execution pipeline;

a DRAM, coupled to the processor;

[an execution pipeline; ]

a digital throttle to estimate a power state, responsive to activity of the execution pipeline;

[a logic to change a frequency of a first Phase Locked Loop clock within a single clock cycle based on the power state.] ; and

a clock unit to generate a first Phase Locked Loop(PLL) clock for a first power state and a

second Phase Locked Loop clock for a second power state; adjusting a voltage and a frequency of a processor based at least in part on the first or second power state and to change a frequency of the first Phase Locked Loop clock within a single clock cycle based on a processor utilization and to change a frequency of the second Phase Locked Loop clock after a completion of a PLL relock.

16. (original) The system of claim 15 wherein the digital throttle comprises an activity monitor to provide an activity level response to activity states of units of the execution pipeline.

17. (new) A processor comprising:

an execution pipeline;

a digital throttle to estimate a power state, responsive to activity of the execution pipeline; and

a clock unit to generate a first Phase Locked Loop(PLL) clock for a first power state and a second Phase Locked Loop clock for a second power state,

and to adjust a voltage and a frequency of a processor based at least in part on the first or second power state and to change a frequency of the first Phase Locked Loop clock within a single clock cycle based on a processor utilization and to change a frequency of the second Phase Locked Loop clock after a completion of a PLL relock.

18. (new) The processor of claim 17 wherein the digital throttle comprises an activity monitor to provide an activity level response to activity states of units of the execution pipeline.

19. (new) A clock generation unit for a processor comprising:

the clock generation unit to generate a first Phase Locked Loop(PLL) clock for a first power state and a second Phase Locked Loop clock for a second power state; adjusting a voltage and a frequency of a processor based at least in part on the first or second power state and to change a frequency of the first Phase Locked Loop clock within a single clock cycle based on the processor utilization and to change a frequency of the second Phase Locked Loop clock after a completion of a PLL relock.

20. (new) A clock generation unit for a processor of claim 18 wherein the clock generation unit gates at least one clock to the processor to control power delivery of a functional unit of the processor.